An Accurate Design Algorithm for *LLC* Resonant Converters—Part I

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***Abstract*—This paper proposes a new approach to optimally design *LLC* converters. The core of the proposed approach is an accurate algorithm that can find all the possible designs satisfying the peak gain requirement. Designers can conveniently evaluate several design results and find the optimal one for their respective applications. Part I of this paper proposes the accurate design algorithm, which is developed based on time-domain resonant waveforms, law of charge conservation, and conservation of energy. Design procedures are also provided for computer automation.**

***Index Terms*—*LLC* converter, modeling, resonant power conversion, switched-mode power supply.**

I. Introduction

LLC resonant converters have been widely used in different applications for their features of wide input voltage, high efficiency. They are employed to increase the power density of laptop adapters [1], [2], reduce the profile of the power supplies for LCD/LED flat panel TV [3], [4], optimize the LED driving [5], [6], improve the performance of the power supplies for servers [7]–[9], and widen the input voltage range of the battery charger [10] or solar panel power modules [11], [12]. *LLC* topology as well as its derivatives are also adopted in fuel cell [13], [14], transportation [15]–[17] or some other high-voltage high-power applications.

Several design methods have been developed in the past. They can be summarized into three categories: 1) fundamental harmonic approximation (FHA) [18]–[22], 2) FHA with time-domain correction [23]–[25], and 3) time-domain analysis [26]–[31]. An important insight is revealed in [20] that although three component values are to be designed, the characteristics of an *LLC* converter are determined by only two variables: the quality factor of the resonant tank, and the inductance ratio. When these two variables are selected, even at different resonant frequencies, the *LLC* converters will have the same peak gain. As will be further demonstrated in this paper, they will have the same component stresses, and even the same waveform shapes. Therefore, the design of an *LLC* resonant tank has two degrees of freedom.

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Previous design methods for *LLC* converters often use the peak gain requirement and additional conditions to complete a design, such as predefined dead time length [18], [19], [28], operation at no load [18], [25], [28], soft start inrush current [27], secondary-side leakage inductance [20], maximum resonant capacitor voltage [23], normalized switching frequency range [29], short-circuit operation [10], and so on. However, when the design objective is efficiency optimization, these additional conditions impose unnecessary restrictions and exclude possible design candidates. For example, the predefined dead time and presumed MOSFET junction capacitance dictates the resonant current at the turn-off point, which in turn dictates the parallel inductance value, but in reality, the dead time length can be selected according to the parallel inductance value; the operation at no load determines the selection of inductance ratio, but in fact, burst-mode operation can solve this problem without compromising resonant tank design [32]–[34]; similarly, some soft-start methods and overcurrent protection methods do not affect the resonant tank design [35].

A further drawback of using preassumed values such as dead time and MOSFET junction capacitance in design steps is that the assumptions may not hold in the final design, which create loops in decision making. For example, if a designer preassumes a relatively long dead time, the resonant current angle of the final design may not provide the assumed dead time; if the designer preassumes a relatively short dead time, the parallel inductance may be unnecessarily small and thus sacrifice efficiency. Also, as will be shown in Part II of this paper, for high-power applications, if use zero-voltage switching (ZVS) requirement to design parallel inductance value, the required peak gain may not be achievable. Similarly, if the final design chooses a different MOSFET from the preassumed one, the ZVS requirement is changed; therefore, the optimal design for the new MOSFET will be different from the existing one. As can be seen above, the search for optimal design becomes an endless loop. The design process is not straightforward.

The above-discussed problem is further complicated by the tradeoff in component selection. For example, larger MOSFETs have lower $R_{\mathrm{ds(on)}}$ but higher junction capacitance and gate charge. The low $R_{\mathrm{ds(on)}}$ can reduce conduction loss, but the high junction capacitance requires increased parallel inductance current to achieve ZVS, which increases conduction loss. Also, the high gate charge slows down the switching and thus increases the required dead time length. The optimal MOSFET selection is a part of the optimal design and must be considered when designing the *LLC* resonant tank values. This causes a loop in the decision making. Similarly, the component tradeoff is even

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more complicated when considering magnetic design. Different resonant frequencies and inductance values have impact on core material selection, air gap length, and leakage inductance, which in turn has impact on efficiency. The magnetic design is a part of the optimal design and should be considered when designing the *LLC* resonant tank values. This again causes a loop in decision making.

When all of the above factors are taken into consideration in searching for an optimal design, existing design methods are incompetent, because the approach they take is to mix all restrictions together, and try to find a single solution. Some restrictions are rather arbitrary, so the solution will not be optimal. More importantly, the problem becomes too large to solve. Two key considerations—peak gain point and resonant current waveform—do not have closed-form solutions in some operation modes. As a result, there is no closed-form formula to find the optimal design. A large number of trial and errors are inevitable in the design process.

One approach to tackle the above problem is to develop an ultimate computer program that take into account everything and conduct a global search for an optimal design [31]. However, the complexity of the mathematical model increases exponentially with the number of factors considered. Especially, when considering parasitic and nonlinear components, the mathematical model can never be as accurate and flexible as simulation. In addition, different applications have different restrictions and preferences. It is almost impossible to develop one program to serve all.

The proposed approach to solve the optimal design problem is to decouple the problems. Mathematical model and simulation tool can be used together to solve each subproblem efficiently. The first step is to find all the possible designs that have the required peak gain, without using any arbitrary assumptions. In this step, the design candidates are narrowed down from virtually unlimited to a handful. The second step is to conduct loss analysis, ZVS evaluation, and include other design restrictions to find the optimal design. Since the candidate resonant tank values are already given in the first step, simulation tool can be used to get accurate evaluation results. For example, one can use simulation tools to evaluate several MOSFETs in a few candidate resonant tank designs. The design effort can be greatly reduced comparing to methods that involve global search and endless decision-making loops.

At the core of the above-mentioned design approach is an algorithm that can accurately find all the candidate designs that meet the peak gain requirement. According to the two-degree-of-freedom insight discussed above, there will be many design candidates—combinations of inductance ratio and quality factor—that meet the peak gain requirement. Each design candidate provides a different performance tradeoff between nominal and worst-case operating conditions. The optimal design for a particular application should exist among the candidates. The selection should be based on loss analysis, but the difficulty is how to find the design candidates. It has been agreed that FHA has large error in predicting the peak gain [19], [20], [25], [27], [28], [30]. Instead, simulation is much more accurate. In [20], a peak gain versus quality factor versus inductance ratio graph is generated using simulation approach. However, an application may have candidates beyond the graph (e.g., very large gain or very small quality factor), and then, the graph will be inadequate. In [30], the peak gain point of a given *LLC* converter can be mathematically estimated through curve-fitting and linear approximation techniques. But the method cannot search for all possible designs based on specified peak gain value and power level.

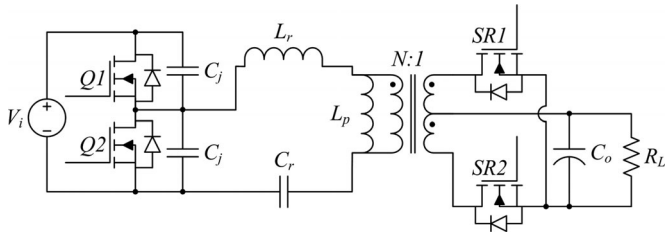

Fig. 1. Topology of the *LLC* Converter.

Part I of this paper will propose an accurate algorithm to find all possible *LLC* converter designs that can provide the exactly required peak gain. Part II of this paper will investigate use of the proposed algorithm in different application scenarios, discuss further insight of the design results, and provide a design procedure. The sections in Part I are organized as follows: Section II introduces operation modes and design variables. Section III discusses the physical relations that will be used in derivation. Sections IV and V derive mathematical solutions for the peak-gain point waveform and the design procedures. Section VI verifies the accuracy of the proposed algorithm. Section VII concludes Part I of this paper.

II. Operation Modes and Design Variables

A. Definition of Operation Modes and Time Points

The topology of the *LLC* converter is illustrated in Fig. 1. The *LLC* resonant tank consists of a resonant inductor L_r, a resonant capacitor C_r, and a parallel inductor L_p in parallel with the load. Variable switching frequency is used to regulate the output voltage. The half-bridge inverter applies a square-wave voltage across the *LLC* resonant tank.

In frequency-domain analysis, the output voltage gain can be calculated by the impedances of the resonant tank using FHA [36]. When the resonant current is *lagging* the applied square-wave voltage, the *LLC* resonant tank is inductive. Further increasing the switching frequency will increase the inductive impedance and thus reduce the output voltage gain. Likewise, when the resonant current is *leading* the applied square-wave voltage, the *LLC* resonant tank is capacitive. Further decreasing the switching frequency will increase the capacitive impedance and thus also reduce the output voltage gain. Therefore, the peak gain point occurs when the resonant current is *in phase with* the applied square-wave voltage. In this scenario, the resonant tank impedance is the lowest (only resistive); thus, the output voltage gain reaches the peak.

However, the peak gain value and switching frequency at which the peak gain occurs are difficult to determine using

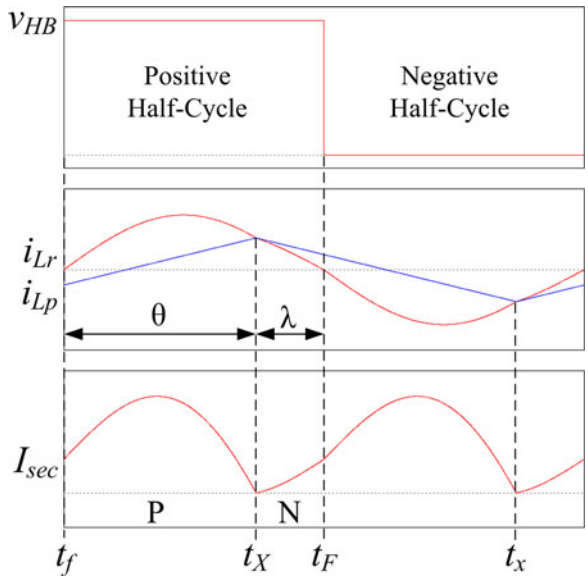

Fig. 2. Waveforms at the peak gain point in PN mode.

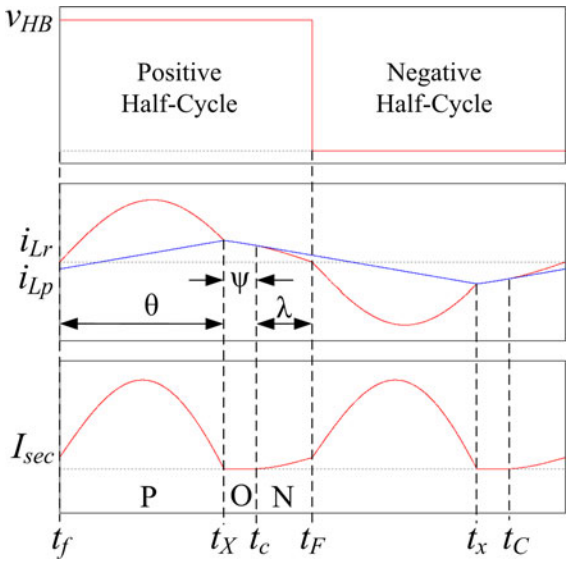

Fig. 3. Waveforms at the peak gain point in PON mode.

frequency-domain analysis, because L_p is periodically clamped by the output capacitor; thus, the operation of resonant tank is nonlinear and variable depending on the operating conditions. The equivalent impedance of the resonant tank is changed accordingly and is difficult to calculate. Therefore, in order to accurately solve the peak gain problem, time-domain analysis is necessary.

In time domain, the peak gain point can be understood from maximum input power point of view. The input power of an *LLC* converter is the product of input voltage, input charge of each switching cycle, and switching frequency. When input voltage reduces, in order to provide the same amount of input power, the per-cycle input charge must increase. The peak gain point occurs when the per-cycle input charge reaches the peak point: further reducing input voltage will cause the maximum input power to reduce. The per-cycle input charge peaks when resonant current is *in phase* with the square-wave input voltage, which is the total equivalent resonant frequency point of the *LLC* resonant tank taking into account the partial resonance of L_p. At the total equivalent resonant frequency point, the amplitude of the resonant current reaches the peak, and so does the per-cycle input charge. Either increasing or decreasing switching frequency will increase reactive input current and thus reduces the per-cycle input charge. Above statements hold true when the switching frequency factor is taken into consideration. This is because near the total equivalent resonant frequency point, the change rate of per-cycle input charge is much greater than the change rate of switching frequency. Therefore, the peak gain point happens at the peak per-cycle input charge point, which is when resonant current is *in phase* with the square-wave input voltage.

Time-domain analysis shows that the *LLC* converter has four operation modes when the output voltage gain is below unity and four operation modes when the output voltage gain is above unity [26]. These operations modes have different naming conventions in [26] and [30]. This paper adopts the naming convention from [30], i.e., use positive–negative (PN) mode and positive-zero-negative (PON) mode to describe the two possible modes at the peak gain point.

TABLE I
DEFINITION OF TIME POINTS

Time point	Definition
t_F	Fall edge of the high-side MOSFET gate.
t_f	Fall edge of the low-side MOSFET gate.
t_X	Extinction point of the output current of a positive half-cycle.
t_x	Extinction point of the output current of a negative half-cycle.
t_C	Conduction point of the output current of a positive half-cycle.
t_c	Conduction point of the output current of a negative half-cycle.

Depending on the design of the resonant tank, the peak gain point may occur in PN or PON mode. The waveforms are shown in Figs. 2 and 3. The definition of time points are summarized in Table I.

In Fig. 2, a full switching cycle of the PN mode is shown. Assuming the dead time is negligible, the half-bridge point voltage ($v_{\rm HB}$) is a square wave, which divides the positive and negative half-cycles. During the positive half-cycle, the output current of the opposite output diode (N interval) begins as soon as the output current of the P interval is extinct. The mode name PN depicts this operation.

In Fig. 3, a full switching cycle of the PON mode is shown. There is an interval with no output current between t_X and t_c (O interval). The mode name PON depicts this operation.

In both Figs. 2 and 3, the resonant current i_{Lr} is zero at t_f and t_F, indicating the operation is at the peak gain point. As will be demonstrated in the next section, each segment of the i_{Lr} waveform is a sinusoidal curve. Therefore, the curve angles at t_f and t_F are *0* and π, respectively. Also, the intervals can be expressed in radians. They are summarized in Tables II and III.

TABLE II
DEFINITION OF INTERVALS IN PN MODE

Interval	Boundary	Time length	Radian
P	From t_f to t_X	t_{fX}	θ
N	From t_X to t_F	t_{XF}	λ

TABLE III
DEFINITION OF INTERVALS IN PON MODE

Interval	Boundary	Time length	Radian
P	From t_f to t_X	t_{fX}	θ
O	From t_X to t_c	t_{Xc}	Ψ
N	From t_c to t_F	t_{cF}	λ

B. Design Variables and Derivation Methodology

The objective of the proposed algorithm is to find all possible designs of L_r, C_r, L_p, which have the exact peak gain value as required. Based on the design results, one can further derive design solutions that have higher peak gain than required; however, unnecessarily high peak gain will compromise the efficiency. Therefore, in most cases, the optimal design has the exact required peak gain value. The proposed algorithm is based on accurate time-domain solution at the peak gain point; therefore, it can push the design parameters to the optimal point closer than existing design methods. The ZVS condition should be verified after all the design solutions are found. This is because the ZVS condition depends on the resonant current (the reversing current at the beginning of each half-cycle); this information is only available after a design solution is given.

The proposed algorithm uses the input voltage range, output voltage, maximum load current, minimum switching frequency, and required peak gain value, which are normally known for a specific design. The minimum switching frequency can be selected based on the available magnetic core size to avoid saturation. Since the efficiency is optimal at the unity gain point, the turns ratio *N* can be chosen accordingly, and then, the peak gain value is determined.

The algorithm derivation is based on equations established using time-domain resonant tank waveforms and insights of charge conservation and energy conservation in *LLC* converters. The basic physical relations used in derivation are discussed in the next section.

III. BASIC PHYSICAL RELATIONS USED IN DERIVATIONS

The basic physical relations in an *LLC* circuit are discussed in this section. They are used in derivations in the following sections.

A. Input Charge and Resonant Capacitor Voltage

The input charge from the input voltage source to the *LLC* power stage usually consists of positive and negative charges due to the reactance of the resonant tank. The net input charge can be calculated from the voltage variation of the series-resonant capacitor over the period at which energy exchange takes place between the input voltage source and the *LLC* power stage. Fig. 4 shows typical waveforms of half-bridge *LLC* converters. The energy exchange period can be identified from the input current waveform i_{Q1}: there is negative input charge from t_f to the zero-crossing point t_o; and there is positive input charge from t_o to t_F. The net input charge can be calculated from the C_r voltage at t_f and t_F, as derived in the following equation:

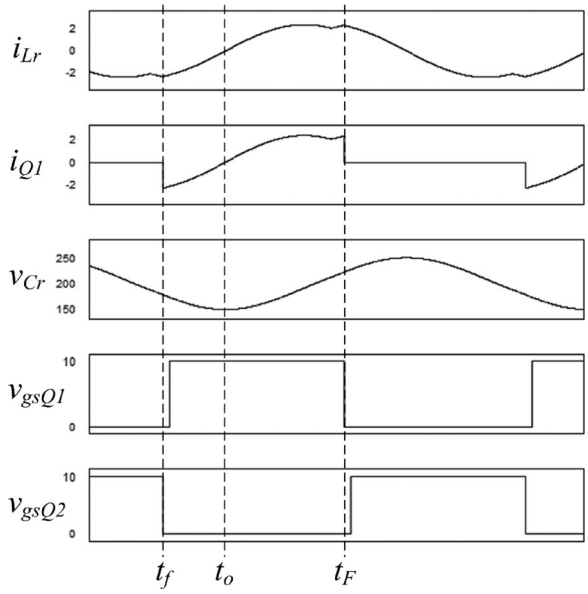

Fig. 4. Typical waveforms of half-bridge *LLC* converters.

$$\begin{aligned} Q_{\text{net}} &= Q_{\text{neg}} + Q_{\text{pos}} \\ &= C_r\left(v_{Cr,\text{to}} - v_{Cr,tf}\right) + C_r\left(v_{Cr,tF} - v_{Cr,\text{to}}\right) \\ &= C_r\left(v_{Cr,tF} - v_{Cr,tf}\right). \end{aligned} \tag{1}$$

For half-bridge *LLC* converters, $v_{Cr,tf}$ and $v_{Cr,tF}$ are symmetrical to a half of the input voltage. Therefore, $v_{Cr,tF}$ can be expressed as a function of $v_{Cr,tf}$ as

$$\frac{V_i}{2} - v_{Cr,tf} = v_{Cr,tF} - \frac{V_i}{2} \Rightarrow v_{Cr,tF} = V_i - v_{Cr,tf}. \tag{2}$$

Combining (1) and (2) gives

$$Q_{\text{net}} = C_r\left(V_i - 2v_{Cr,tf}\right). \tag{3}$$

Assuming 100% efficiency, the input energy in a switching cycle equals the output energy in that switching cycle. The input energy can be derived from the input charge and the input voltage. This relation can be expressed as

$$E_{o,\text{per-cycle}} = \frac{V_o^2}{R_L f_s} = V_i Q_{\text{net}}. \tag{4}$$

Combining (3) and (4) gives

$$v_{Cr,tf} = \frac{C_r R_L V_i^2 f_s - V_o^2}{2R_L f_s C_r V_i}. \tag{5}$$

The minimum switching frequency occurs at minimum input voltage and full load. According to (5), v_{Cr} at t_f and the C_r

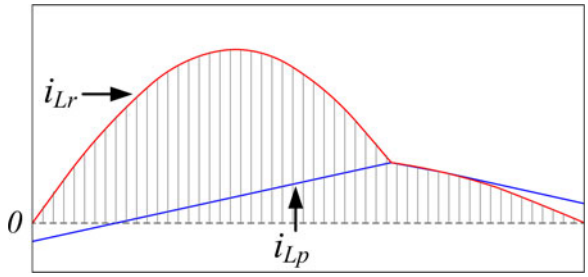

Fig. 5. Input charge derived from the resonant current waveform.

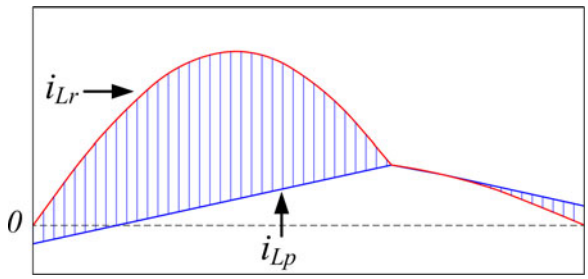

Fig. 6. Output charge derived from the resonant current waveform.

value have a relation described in (6). In (4) and (5), R_L represents load resistance in general. For concise presentation, from (6) and onwards, R_L represents the full-load resistance

$$v_{Cr,tf} = \frac{C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2}{2R_L f_{s,\min} C_r V_{i,\min}}. \tag{6}$$

Equation (3) does not count for the input charge resulted from the MOSFET junction capacitance. It is so because the resonant current is zero at t_f and t_F; thus, ZVS is completely lost, and the energy in the junction capacitance is completely dissipated as switching loss. More details about this physical relation are discussed in [37].

B. Input Charge and Resonant Current

In a half-bridge *LLC* converter, the energy exchange between the input voltage source and the *LLC* power stage only occurs in the positive half-cycles. Therefore, the input charge of each switching cycle can be derived from the area under the resonant current waveform i_{Lr} in a positive half-cycle (which is also the input current), as shown in the shadowed area in Fig. 5. Assuming 100% efficiency, in steady state, the input energy calculated from the input charge equals the output energy of the entire switching cycle.

C. Output Charge and Resonant Current

The instant output current of the *LLC* resonant tank (on the primary side) is the difference of i_{Lr} and i_{Lp}. Therefore, the output charge of each half-cycle (reflected to the primary side) equals the area bounded by the i_{Lr} and the i_{Lp} waveforms, as shown in the shadowed area in Fig. 6.

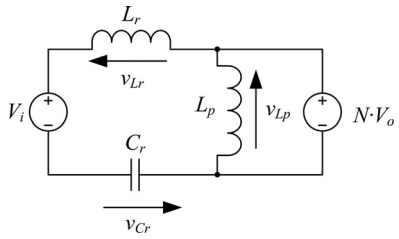

Fig. 7. Equivalent circuit for the P interval.

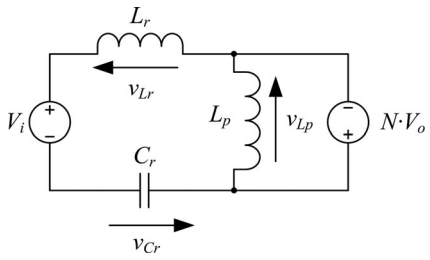

Fig. 8. Equivalent circuit for the N interval.

IV. Design Algorithm Derivation (PN Mode)

This section derives the design algorithm when the peak gain point happens in the PN mode.

A. Derivation

The variables used in the derivations are summarized in (7) for quick reference. N is the transformer turns ratio. N_p is the primary turns, and N_s is the secondary turns. K is the inductance ratio. $\omega_{s,\min}$ is the minimum switching frequency in radians. ω_r is the resonant frequency of L_r and C_r, in radians. ω_p is the resonant frequency of L_p, L_r, and C_r, in radians

$$N = \frac{N_p}{N_s}, K = \frac{L_p}{L_r}, \quad \omega_{s,\min} = 2\pi f_{s,\min},$$
$$\omega_r = \frac{1}{\sqrt{L_r C_r}}, \quad \omega_p = \frac{1}{\sqrt{(L_r + L_p)C_r}}. \tag{7}$$

1) Kirchhoff's Voltage Law (KVL) Equations: In PN mode, L_p is clamped by the output capacitor in both P and N intervals. The waveforms are shown in Fig. 2. The equivalent circuit of the P interval is shown in Fig. 7. The equivalent circuit of the N interval is shown in Fig. 8. Using KVL, the differential equations of the two intervals are derived in (8) and (9), respectively.

For P interval

$$L_r C_r \frac{d^2}{dt^2} v_{Cr} + v_{Cr} = V_{i,\min} - NV_o. \tag{8}$$

For N interval

$$L_r C_r \frac{d^2}{dt^2} v_{Cr} + v_{Cr} = V_{i,\min} + NV_o \tag{9}$$

where $V_{i,\min}$ is the minimum input voltage, which is corresponding to the peak gain point operation.

The general solution for (8) is given in (10), where k_1 and k_2 are coefficients, which are determined by the initial condition

$$v_{Cr}(t) = k_1 \cos(\omega_r t) + k_2 \sin(\omega_r t) + V_{i,\min} - NV_o. \quad (10)$$

From (10), the general solution for the resonant current can be derived as

$$i_{Lr}(t) = C_r \omega_r \left[-k_1 \sin(\omega_r t) + k_2 \cos(\omega_r t)\right]. \quad (11)$$

Similarly, the general solution for (9) is given in (12), where k_5 and k_6 are coefficients, which are determined by the initial condition

$$v_{Cr}(t) = k_5 \cos(\omega_r t) + k_6 \sin(\omega_r t) + V_{i,\min} + NV_o. \quad (12)$$

From (12), the general solution for the resonant current can be derived as

$$i_{Lr}(t) = C_r \omega_r \left[-k_5 \sin(\omega_r t) + k_6 \cos(\omega_r t)\right]. \quad (13)$$

2) Initial Conditions: At t_f, the resonant current i_{Lr} is zero, and the C_r voltage is expressed by (6). To solve for the initial condition, t is substituted by 0 in (10) and (11). Then, the coefficients k_1 and k_2 can be solved as

$$k_1 = \frac{2NC_r R_L V_o V_{i,\min} f_{s,\min} - C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2}{2R_L f_{s,\min} C_r V_{i,\min}}. \quad (14)$$

$$k_2 = 0. \quad (15)$$

At t_F, the resonant current is also zero, and the C_r voltage is expressed by combining (2) and (6). To solve for the initial condition, t is substituted by 0 in (12) and (13). Then, the coefficients k_5 and k_6 can be solved as

$$k_5 = \frac{2NC_r R_L V_o V_{i,\min} f_{s,\min} + C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2}{-2R_L f_{s,\min} C_r V_{i,\min}} \quad (16)$$

$$k_6 = 0. \quad (17)$$

3) θ and λ Values: According to the definitions in Table II, θ and λ have relations with time length

$$\theta = \omega_r t_{fX} \quad (18)$$

$$\lambda = \omega_r t_{XF}. \quad (19)$$

Then, the circuit state at t_X can be derived from the initial condition at t_f by substituting (14), (15), and $\omega_r t = q$ into (10) and (11)

$$v_{Cr,tX} = \frac{\left(2NC_r R_L V_o V_{i,\min} f_{s,\min} - C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2\right)\cos(\theta)}{2R_L f_{s,\min} C_r V_{i,\min}} + V_{i,\min} - NV_o \quad (20)$$

$$i_{Lr,tX} = -\frac{\left(2NC_r R_L V_o V_{i,\min} f_{s,\min} - C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2\right)\sin(\theta)}{2R_L f_{s,\min} V_{i,\min}\sqrt{L_r C_r}}. \quad (21)$$

Also, the circuit state at t_X can be derived from the initial condition at t_F by substituting (16), (17), and $\omega_r t = -\lambda$ into (12) and (13)

$$v_{Cr,tX} = \frac{\left(2NC_r R_L V_o V_{i,\min} f_{s,\min} + C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2\right)\cos(-\lambda)}{-2R_L f_{s,\min} C_r V_{i,\min}} + V_{i,\min} + NV_o \quad (22)$$

$$i_{Lr,tX} = \frac{\left(2NC_r R_L V_o V_{i,\min} f_{s,\min} + C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2\right)\sin(-\lambda)}{R_L f_{s,\min} V_{i,\min}\sqrt{L_r C_r}}. \quad (23)$$

Connecting (20) and (22) can solve for cos(λ): equation (24) as shown at the bottom of the page.

Connecting (21) and (23) can solve for sin(λ)

$$\sin(\lambda) = \frac{\left(2NC_r R_L V_o V_{i,\min} f_{s,\min} - C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2\right)\sin(\theta)}{2NC_r R_L V_o V_{i,\min} f_{s,\min} + C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2}. \quad (25)$$

From (24) and (25), θ has an analytical solution

$$\theta = \arccos\left(\frac{V_{i,\min}\left(4N^2 C_r R_L V_o f_{s,\min} - 2NC_r R_L V_{i,\min} f_{s,\min} + V_o\right)}{2N\left(2NC_r R_L V_o V_{i,\min} f_{s,\min} - C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2\right)}\right). \quad (26)$$

From (25) and (26), λ also has an analytical solution

$$\lambda = \arcsin\left(\frac{\left(2NC_r R_L V_o V_{i,\min} f_{s,\min} - C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2\right)\sin(\theta)}{2NC_r R_L V_o V_{i,\min} f_{s,\min} + C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2}\right). \quad (27)$$

C_r is treated as a known value in (26) and (27). As will be discussed in Section IV-B, the initial C_r value is selected

$$\cos(\lambda) = -\frac{2N\cos(\theta) C_r R_L V_o V_{i,\min} f_{s,\min} - 4NC_r R_L V_o V_{i,\min} f_{s,\min} - \cos(\theta) C_r R_L V_{i,\min}^2 f_{s,\min} - \cos(\theta) V_o^2}{2NC_r R_L V_o V_{i,\min} f_{s,\min} + C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2} \quad (24)$$

based on component stress and then increases with an arbitrary interval after each iteration. Each C_r value results in a set of L_r and L_p values which provide critically designed peak gain. The iteration continues until the boundary between PN and PON modes is reached.

4) K Value: L_p is clamped by the output capacitor in both P and N intervals; therefore, its current slope is linear. The L_p current at t_f and t_F are symmetrical. Also, the L_p current and L_r current are equal at t_X. Above relations can be described as follows:

$$i_{Lp,tF} + \frac{NV_o\lambda}{L_p\omega_r} = i_{Lr,tX} \tag{28}$$

$$i_{Lp,tf} + \frac{NV_o\theta}{L_p\omega_r} = i_{Lr,tX} \tag{29}$$

$$i_{Lp,tf} = -i_{Lp,tF}. \tag{30}$$

Combining (21) and (28)–(30), after manipulation, the analytical solution of *K* is derived as

$$K = \frac{-NC_rR_LV_oV_{i,\min}f_{s,\min}(\lambda+\theta)}{\left(2NC_rR_LV_oV_{i,\min}f_{s,\min} - C_rR_LV_{i,\min}^2f_{s,\min} - V_o^2\right)\sin(\theta)}. \tag{31}$$

5) Inductor Values: The total time length of the positive and negative intervals equals to half switching period. This relation is described in (32). Then, the analytical solution for ω_r can be derived in (33)

$$\frac{\lambda+\theta}{\omega_r} = \frac{1}{2f_{s,\min}} \tag{32}$$

$$\omega_r = 2\lambda f_{s,\min} + 2\theta f_{s,\min}. \tag{33}$$

Because C_r is a known value, L_r and L_p can be solved as follows:

$$L_r = \frac{1}{C_r\omega_r^2} \tag{34}$$

$$L_p = KL_r. \tag{35}$$

6) Checking $v_{Cr,tX}$ Margin: At t_X, the output current of the positive half-cycle is extinct; thus, there is no flux linkage between the primary and secondary sides. Hence, the output voltage source shown in Fig. 7 is removed from the equivalent circuit; thus, L_p is no longer clamped, and the two inductors proportionally divide the total voltage that is applied on them, which is the difference of V_i and v_{Cr}. In PN and PON modes, $v_{Cr,tX}$ is higher than V_i; thus, the voltage on the inductors is negative. If the negative voltage at t_X across L_p exceeds $-NV_o$, the output current of the N interval will immediately conduct, and the operation is in PN mode. If $v_{Cr,tX}$ is not high enough to conduct output current of the N interval, an O interval exists, and the operation is in PON mode. The design procedure developed in this section is only valid in PN mode. Therefore, it is necessary to check the design results using the $v_{Cr,tX}$ criterion.

The mathematical expression of the above-described relation is in (36), where NV_o is the voltage across L_p required to conduct output current. The margin of $v_{Cr,tX}$ before entering PON mode is expressed in (37)

$$v_{Cr,tX} - V_{i,\min} > \frac{NV_o(K+1)}{K} \tag{36}$$

$$v_{Cr,tX,\mathrm{margin}} = v_{Cr,tX} - V_{i,\min} - \frac{NV_o(K+1)}{K}. \tag{37}$$

Substituting (20) into (37) gives

$$v_{Cr,tX,\mathrm{margin}} = \frac{\left(2NC_rR_LV_oV_{i,\min}f_{s,\min} - C_rR_LV_{i,\min}^2f_{s,\min} - V_o^2\right)\cos(\theta)}{2R_Lf_{s,\min}C_rV_{i,\min}} - NV_o - \frac{NV_o(K+1)}{K}. \tag{38}$$

When the margin is less than 0, the design result is invalid, and the design search should continue in PON mode.

B. Design Procedure

The design search procedure in PN mode is described as follows.

1) Determine the smallest C_r value as a starting point of the design search. The smallest C_r value is determined by its component voltage rating. The reason is below. When operating at the peak gain point, the resonant current changes polarity at t_F; therefore, the C_r voltage at t_F is also its peak voltage. Using (2) and (6), the relation of the C_r value and $v_{Cr,tF}$ can be derived in (39), where $v_{Cr,\mathrm{rating}}$ is the capacitor voltage rating, which is also the highest $v_{Cr,tF}$. If the capacitor is not selected beforehand, a rough value can used, e.g., 1 kV
$$C_{r,\min} = \frac{V_o^2}{R_Lf_{s,\min}(2v_{Cr,\mathrm{rating}} - V_{i,\min})V_{i,\min}}. \tag{39}$$
2) Use (26) and (27) to calculate θ and λ, respectively.
3) Use (31) to calculate *K*.
4) Use (33)–(35) to calculate L_r and L_p, respectively.
5) Check the validity of the design results (positive and real). Use (38) to check the $v_{Cr,tX}$ margin. If the results are invalid, or the margin is less than 0, it means the design research in PN mode is completed. If the results are valid and the margin is greater than 0, continue to Step 6.
6) Increase C_r value by a small step, e.g., 1 nF, and repeat steps 2–5.

V. Design Algorithm Derivation (PON Mode)

This section derives the design algorithm when the peak gain point happens in the PON mode.

A. Derivation

1) KVL Equations: In PON mode, L_p is clamped by the output capacitor during P and N intervals, but participate in the resonance during the O interval. The waveforms are shown in Fig. 3. The equivalent circuits for the P and the N intervals are shown in Figs. 7 and 8, respectively. The equivalent circuit for

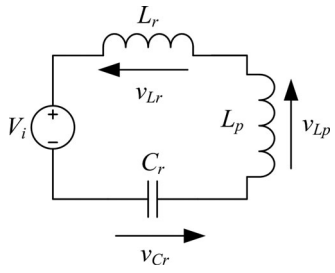

Fig. 9. Equivalent circuit of the O interval.

the O interval is shown in Fig. 9. Using KVL, the differential equations of the P and the N intervals are derived in (8) and (9), respectively, and the differential equation of the O interval is derived as

$$(L_r + L_p)C_r \frac{d^2}{dt^2} v_{Cr}(t) + v_{Cr}(t) = V_{i,\min}. \tag{40}$$

The general solution for (40) is given in (41), where k_3 and k_4 are coefficients, which are determined by the initial condition

$$v_{Cr}(t) = k_3 \cos(\omega_p t) + k_4 \sin(\omega_p t) + V_{i,\min}. \tag{41}$$

From (41), the general solution for the resonant current can be derived as

$$i_{Lr}(t) = C_r \omega_p \left[-k_3 \sin(\omega_p t) + k_4 \cos(\omega_p t)\right]. \tag{42}$$

2) Initial Conditions: The initial conditions at t_f and t_F can be solved the same way as in PN mode. The solutions for k_1, k_2, k_5, and k_6 are in (14)–(17), respectively.

The circuit state at t_X can be derived the same way as in PN mode. The solutions are in (20) and (21).

The circuit state at t_X can be also derived by substituting $t =$ 0 into (41) and (42) as

$$v_{Cr,tX} = k_3 + V_{i,\min} \tag{43}$$

$$i_{Lr,tX} = C_r k_4 \omega_p. \tag{44}$$

By connecting (20) and (43), and (21) and (44), respectively, the expressions of k_3 and k_4 are derived as equation 45 and 46 as shown at the bottom of the page.

3) Expression of K: The circuit state at t_c can be derived from the initial condition at t_F by substituting (16), (17), and $\omega_r t = --l$ into (12) and (13)

$$v_{Cr,tc} = \frac{\left(2NC_r R_L V_o V_{i,\min} f_{s,\min} + C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2\right)\cos(-\lambda)}{-2R_L f_{s,\min} C_r V_{i,\min}} + V_{i,\min} + NV_o \tag{47}$$

$$i_{Lr,tc} = \frac{\left(2NC_r R_L V_o V_{i,\min} f_{s,\min} + C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2\right)\sin(-\lambda)}{2R_L f_{s,\min} V_{i,\min}\sqrt{L_r C_r}}. \tag{48}$$

L_p is clamped by the output capacitor in P and N intervals; therefore, its current slope is linear. The L_p current at t_f and t_F are symmetrical. Also, the L_p current and L_r current are equal at t_X and t_c, respectively. Above relations can be described as

$$i_{Lp,tf} + \frac{NV_o\theta}{L_p\omega_r} = i_{Lr,tX} \tag{49}$$

$$i_{Lp,tF} + \frac{NV_o\lambda}{L_p\omega_r} = i_{Lr,tc} \tag{50}$$

$$i_{Lp,tF} = -i_{Lp,tf}. \tag{51}$$

Substituting (21) into (49) gives the expression of $i_{Lp,tf}$

$$i_{Lp,tf} = \frac{\left(2NC_r R_L V_o V_{i,\min} f_{s,\min} - C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2\right)\sin(\theta)}{-2R_L f_{s,\min} V_{i,\min}\sqrt{L_r C_r}} - \frac{NV_o\theta\sqrt{L_r C_r}}{KL_r}. \tag{52}$$

Substituting (48) and (51) into (50) also gives the expression of $i_{Lp,tf}$

$$i_{Lp,tf} = \frac{\left(2NC_r R_L V_o V_{i,\min} f_{s,\min} + C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2\right)\sin(\lambda)}{2R_L f_{s,\min} V_{i,\min}\sqrt{L_r C_r}} + \frac{NV_o\lambda\sqrt{L_r C_r}}{KL_r}. \tag{53}$$

Connecting (52) and (53), and after manipulation, the expression of K is derived as

$$k_3 = \frac{2N\cos(\theta) C_r R_L V_o V_{i,\min} f_{s,\min} - 2NC_r R_L V_o V_{i,\min} f_{s,\min} - \cos(\theta) C_r R_L V_{i,\min}^2 f_{s,\min} - \cos(\theta) V_o^2}{2R_L f_{s,\min} C_r V_{i,\min}} \tag{45}$$

$$k_4 = \frac{\sqrt{L_r(K+1)C_r}\sin(\theta)\left(2NC_r R_L V_o V_{i,\min} f_{s,\min} - C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2\right)}{-2C_r R_L f_{s,\min} V_{i,\min}\sqrt{L_r C_r}} \tag{46}$$

$$K = \frac{-2NC_r R_L V_o V_{i,\min} f_{s,\min}(\lambda+\theta)}{\begin{array}{l}2N\sin(\theta) C_r R_L V_o V_{i,\min} f_{s,\min} + 2N\sin(\lambda) C_r R_L V_o V_{i,\min} f_{s,\min} \\ -\sin(\theta) C_r R_L V_{i,\min}^2 f_{s,\min} + \sin(\lambda) C_r R_L V_{i,\min}^2 f_{s,\min} - \sin(\theta) V_o^2 - \sin(\lambda) V_o^2\end{array}} \tag{54}$$

4) C_r Voltage at t_c: As discussed in Section IV-A6, at t_c, the C_r voltage is on the edge to conduct the output current. This relation can be described as

$$v_{Cr,tc} = V_{i,\min} + NV_o\left(\frac{K+1}{K}\right). \tag{55}$$

Substituting (47) and (54), shown at the bottom of the previous page, into (55) yields an equation of θ and λ, written as

$$\begin{aligned}
&-2NC_rR_LV_oV_{i,\min}f_{s,\min}\cos(\lambda)\lambda\\
&-2NC_rR_LV_oV_{i,\min}f_{s,\min}\cos(\lambda)\theta\\
&+2N\sin(\theta)C_rR_LV_oV_{i,\min}f_{s,\min}\\
&+2N\sin(\lambda)C_rR_LV_oV_{i,\min}f_{s,\min}\\
&-C_rR_LV_{i,\min}^2f_{s,\min}\cos(\lambda)\lambda\\
&-C_rR_LV_{i,\min}^2f_{s,\min}\cos(\lambda)\theta\\
&-\sin(\lambda)V_o^2-\sin(\theta)C_rR_LV_{i,\min}^2f_{s,\min}\\
&+\sin(\lambda)C_rR_LV_{i,\min}^2f_{s,\min}\\
&+V_o^2\cos(\lambda)\lambda+V_o^2\cos(\lambda)\theta-\sin(\theta)V_o^2=0.
\end{aligned} \tag{56}$$

5) Input and Output Charge: As discussed in Section III-B, the input charge of a switching cycle can be derived from the integral of the input current during a positive half-cycle. In PON mode, this relation is illustrated in Fig. 5 and expressed in (57). On the right-hand side of the equation, the $i_{Lr}(t)$ in the first term is defined in (11); the $i_{Lr}(t)$ in the third term is defined in (13)

$$Q_{\text{in}} = \int_0^{\frac{\theta}{\omega_r}} i_{Lr}(t)dt + (v_{Cr,tc} - v_{Cr,tX})C_r + \int_{\frac{-\lambda}{\omega_r}}^0 i_{Lr}(t)dt. \tag{57}$$

Also, as discussed in Section III-C, the output charge of the *LLC* resonant tank during a half-cycle can be derived from the difference of i_{Lr} and i_{Lp} waveforms. In PON mode, this relation is illustrated in Fig. 6 and expressed in (58). On the right-hand side of the equation, the $i_{Lr}(t)$ in the first term is defined in (11); the $i_{Lr}(t)$ in the fourth term is defined in (13)

$$\begin{aligned}
Q_{\text{out,half-cycle}} &= \int_0^{\frac{\theta}{\omega_r}} i_{Lr}(t) - i_{Lp,tf}dt - \frac{NV_o}{2L_p}\left(\frac{\theta}{\omega_r}\right)^2\\
&+i_{Lr,tc}\frac{\lambda}{\omega_r} - \int_{\frac{-\lambda}{\omega_r}}^0 i_{Lr}(t)dt - \frac{NV_o}{2L_p}\left(\frac{\lambda}{\omega_r}\right)^2.
\end{aligned} \tag{58}$$

Assuming there is no power loss, (57) and (58) can be connected by the law of conservation of energy. The relation can be expressed as

$$Q_{\text{out,half-cycle}}NV_o = \frac{1}{2}Q_{\text{in}}V_{i,\min}. \tag{59}$$

Substitute (6), (14)–(17), (20), (48), (53)–(55), (57), and (58) into (59), and after complicated mathematical manipulation, an equation of θ and λ can be derived as

$$\begin{aligned}
&4(2N\sin(\theta)\lambda C_rR_LV_oV_{i,\min}f_{s,\min}\\
&+2N\sin(\theta)\theta C_rR_LV_oV_{i,\min}f_{s,\min}\\
&-2N\sin(\lambda)\lambda C_rR_LV_oV_{i,\min}f_{s,\min}\\
&-2N\sin(\lambda)\theta C_rR_LV_oV_{i,\min}f_{s,\min}\\
&+4N\cos(\theta)C_rR_LV_oV_{i,\min}f_{s,\min}\\
&-4NC_rR_LV_oV_{i,\min}f_{s,\min}\cos(\lambda)\\
&-\sin(\theta)\lambda C_rR_LV_{i,\min}^2f_{s,\min}\\
&-\sin(\theta)\theta C_rR_LV_{i,\min}^2f_{s,\min}\\
&-\sin(\lambda)\lambda C_rR_LV_{i,\min}^2f_{s,\min}\\
&-\sin(\lambda)\theta C_rR_LV_{i,\min}^2f_{s,\min}\\
&-2\cos(\theta)C_rR_LV_{i,\min}^2f_{s,\min}\\
&-2C_rR_LV_{i,\min}^2f_{s,\min}\cos(\lambda)\\
&+4C_rR_LV_{i,\min}^2f_{s,\min}-\sin(\theta)\lambda V_o^2\\
&-\sin(\theta)\theta V_o^2+\sin(\lambda)\lambda V_o^2\\
&+\sin(\lambda)\theta V_o^2-2\cos(\theta)V_o^2\\
&+2V_o^2\cos(\lambda))NV_oR_Lf_{s,\min}(\lambda+\theta)\\
&-4(2NC_rR_LV_oV_{i,\min}f_{s,\min}\cos(\lambda)\lambda\\
&+2NC_rR_LV_oV_{i,\min}f_{s,\min}\cos(\lambda)\theta\\
&-2N\sin(\theta)C_rR_LV_oV_{i,\min}f_{s,\min}\\
&-2N\sin(\lambda)C_rR_LV_oV_{i,\min}f_{s,\min}\\
&+C_rR_LV_{i,\min}^2f_{s,\min}\cos(\lambda)\lambda\\
&+C_rR_LV_{i,\min}^2f_{s,\min}\cos(\lambda)\theta\\
&+\sin(\theta)C_rR_LV_{i,\min}^2f_{s,\min}\\
&-\sin(\lambda)C_rR_LV_{i,\min}^2f_{s,\min}\\
&-V_o^2\cos(\lambda)\lambda-V_o^2\cos(\lambda)\theta+\sin(\theta)V_o^2\\
&+\sin(\lambda)V_o^2+2\lambda V_o^2+2\theta V_o^2)\\
&R_Lf_{s,\min}V_{i,\min}=0.
\end{aligned} \tag{60}$$

Equation (56) and (60) are both nonlinear functions of θ and λ. They can be numerically solved by 2-D Newton's method as that used in MATLAB.

C_r is treated as a known value in (56) and (60). As will be discussed in Section V-B, the initial C_r value is from the last C_r value used in the PN mode and then increases with an arbitrary interval after each iteration. Each C_r value results in a set of L_r and L_p values which provide critically designed peak gain. The iteration continues until no solution can be found, which means all C_r values in PON mode have been swept.

6) Solve Ψ: The C_r voltage at t_c can be derived by substituting $\omega_p t = Y$, (43), and (44) into (41). It is also derived in (55).

Connecting the two equations gives equation 61 shown at the bottom of the page

The expression of Ψ can be directly derived from (61) using symbolic tools such as MATLAB and Maple. However, the expression is too large to display in this paper. A place holder (62) is used in the following text to refer to this expression (Please contact authors by email for an electronic copy of this equation):

$$\text{Expression of } \psi, \text{ directly derived from (61).} \tag{62}$$

7) Solve Component Values: According to the definitions in (7), ω_p and ω_r have the following relation:

$$\omega_p = \frac{\omega_r}{\sqrt{K+1}}. \tag{63}$$

The total time length of the three intervals equals to a half switching period. This relation is described in (64). Substituting (63) into (64), the analytical solution for ω_r can be derived in (65)

$$\frac{\lambda+\theta}{\omega_r} + \frac{\psi}{\omega_p} = \frac{1}{2f_{s,\min}} \tag{64}$$

$$\omega_r = 2\psi\sqrt{K+1}f_{s,\min} + 2f_{s,\min}\lambda + 2f_{s,\min}\theta. \tag{65}$$

Because C_r is a known value, L_r and L_p can be solved in (34) and (35), respectively.

8) Check $v_{Cr,tf}$ Margin: In PON mode, the C_r voltage must reach the threshold to conduct the output current before t_f. If the C_r voltage at t_f is still below the threshold, it means the boundary of PON mode is reached. Because the design procedure developed in this section is only valid in PON mode, it is necessary to check the design results using the $v_{Cr,tf}$ criterion.

The mathematical expression of the $v_{Cr,tf}$ criterion is

$$v_{Cr,tf} < -\frac{NV_o\,(K+1)}{K}. \tag{66}$$

Using (6) and (66), the $v_{Cr,tf}$ margin is derived as

$$v_{Cr,tf,\text{margin}} = -\frac{C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2}{2R_L f_{s,\min} C_r V_{i,\min}} - \frac{NV_o\,(K+1)}{K}. \tag{67}$$

When the margin is less than 0, the design result is invalid, indicating that the design search in PON mode is completed.

B. Design Procedure

The design search procedure in PON mode is described as follows.

1) Use the last C_r value that has been failed in the PN mode as the starting point of the PON mode design search. The θ and λ values of the last successful PN mode solution are used as the first set of initial values to solve the PON mode equations.
2) Use 2-D Newton's method to solve the transcendental equation set (56) and (60). For the first iteration, the initial values are from Step 1. For the subsequent iterations, the initial values are from the solutions of the previous iteration.
3) Use (54) to calculate *K*.
4) Use (62) to calculate Ψ.
5) Use (34), (35), and (65) to calculate L_p and L_r.
6) Check the validity of the design results (positive and real). Use (67) to check the $v_{Cr,tf}$ margin. If the results are invalid, or the margin is less than 0, it means the design research in PON mode is completed. If the results are valid and the margin is greater than 0, continue to Step 7.
7) Increase C_r value by a small step, e.g., 1 nF, and repeat steps 2–6.

Step 1 of the above design procedure shows that, even if an *LLC* converter is expected to be designed in PON mode, the calculation should still start from PN mode. This is because the PN mode has a closed-form solution, whereas PON mode involves transcendental equations and thus relies on numerical solution. In order to ensure the robustness of the proposed algorithm—that the numerical solution always converge to the correct point—the last PN mode closed-form solution before the PN/PON boundary is used as the initial condition to calculate the first PON mode numerical solution. For subsequent PON mode calculations, the initial values are the solutions of the previous iteration. This strategy ensures that the proposed algorithm always produce correct numerical results.

VI. Algorithm Verification

The algorithm derived above is automated by MATLAB programming. The execution time of the proposed algorithm to find all possible design candidates is less than 2 s using a Lenovo X200 computer with Intel Core 2 Duo P8600 CPU. Simulation approach is used here to demonstrate the accuracy of the proposed algorithm.

The design specification used for the verification is summarized in Table IV. The design results from the proposed algorithm are listed in Table V.

According to the proposed algorithm, all the design results in Table V should provide 12-V/50-A output power at 280-V input voltage and 100-kHz switching frequency. PSIM simulation software is used to verify the design accuracy of the Design No. 1, 10, 20, and 25. The simulation results are shown in Figs. 10–13.

In Figs. 10–13, the resonant currents cross zero at the exact MOSFETs' switching points, indicating the peak-gain point operation; the average output currents are exactly 50 A. These simulation results demonstrate the accuracy of the proposed

$$\frac{\left(2N\cos(\theta)C_r R_L V_o V_{i,\min} f_{s,\min} - 2NC_r R_L V_o V_{i,\min} f_{s,\min} - \cos(\theta)C_r R_L V_{i,\min}^2 f_{s,\min} - \cos(\theta)V_o^2\right)\cos(\psi)}{2R_L f_{s,\min} C_r V_{i,\min}}$$
$$- \frac{\sqrt{L_r\,(K+1)C_r}\sin(\theta)\left(2NC_r R_L V_o V_{i,\min} f_{s,\min} - C_r R_L V_{i,\min}^2 f_{s,\min} - V_o^2\right)\sin(\psi)}{2C_r R_L f_{s,\min} V_{i,\min}\sqrt{L_r C_r}} + V_{i,\min} = \frac{KNV_o + KV_{i,\min} + NV_o}{K} \tag{61}$$

TABLE IV
SPECIFICATION OF DESIGN EXAMPLE 1

Nominal input voltage	384 V
Minimum input voltage	280 V
Minimum input voltage with ZVS	375 V
Output voltage	12 V
Minimum switching frequency	100 kHz
Full load power	600 W
Transformer turns ratio	16 : 1

TABLE V
DESIGN RESULTS FROM THE PROPOSED ALGORITHM

Design No.	C_r (nF)	L_r (μH)	L_p (μH)	Resonant Frequency (kHz)
1	6	380.9244	111.7068	105.275
2	7	320.2793	113.2521	106.2935
3	8	274.6931	114.9072	107.3622
4	9	239.1382	116.686	108.4862
5	10	210.597	118.6049	109.6716
6	11	187.1482	120.6834	110.9254
7	12	167.5096	122.9453	112.256
8	13	150.7923	125.4199	113.6734
9	14	136.3598	128.1435	115.1895
10	15	123.7436	131.1616	116.8189
11	16	112.5902	134.5183	118.5796
12	17	102.6276	138.118	120.4935
13	18	93.6432	141.9404	122.5874
14	19	85.467	146	124.8948
15	20	77.9608	150.3098	127.458
16	21	71.0102	154.8805	130.3317
17	22	64.5188	159.7177	133.5875
18	23	58.4036	164.8178	137.3208
19	24	52.5925	170.1615	141.6617
20	25	47.0212	175.7023	146.7923
21	26	41.6328	181.3471	152.9733
22	27	36.3778	186.9216	160.5905
23	28	31.2196	192.1061	170.2266
24	29	26.152	196.3064	182.7547
25	30	21.2914	198.3318	199.1394

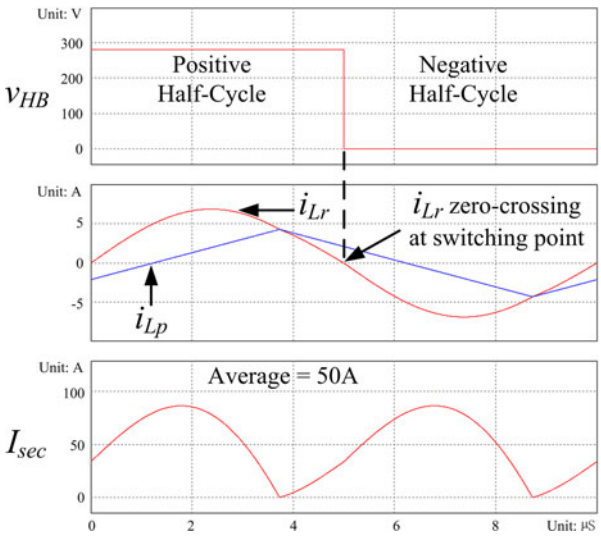

Fig. 10. Peak gain point of Design Example 1. Design No. 1. $V_{\rm in} = 280V$, $V_o = 12$ V, $F_s = 100$ kHz. Output current is exactly 50 A.

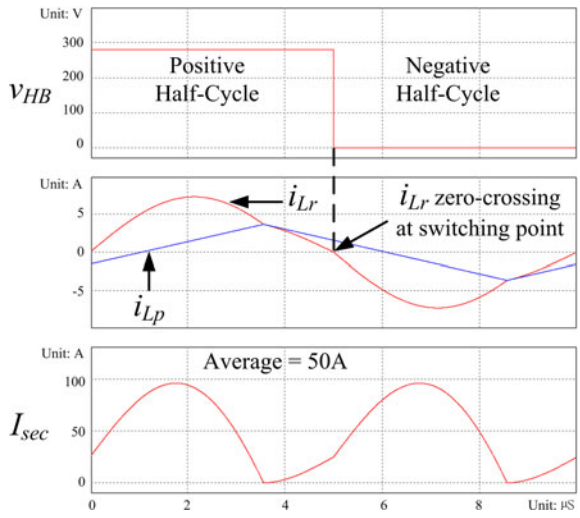

Fig. 11. Peak gain point of Design Example 1. Design No. 10. $V_{\rm in} = 280$ V, $V_o = 12$ V, $F_s = 100$ kHz. Output current is exactly 50 A.

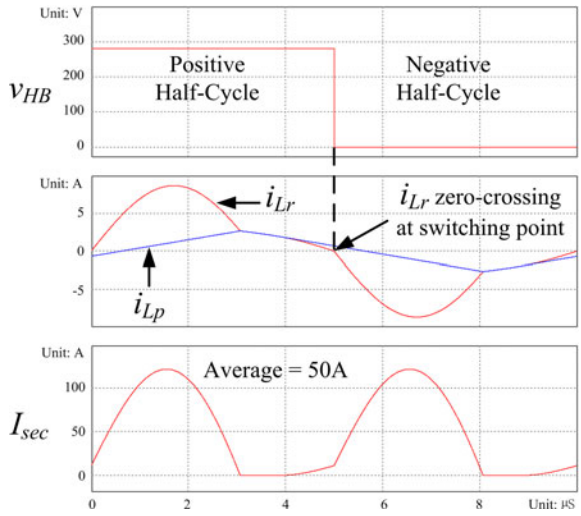

Fig. 12. Peak gain point of Design Example 1. Design No. 20. $V_{\rm in} = 280$ V, $V_o = 12$ V, $F_s = 100$ kHz. Output current is exactly 50 A.

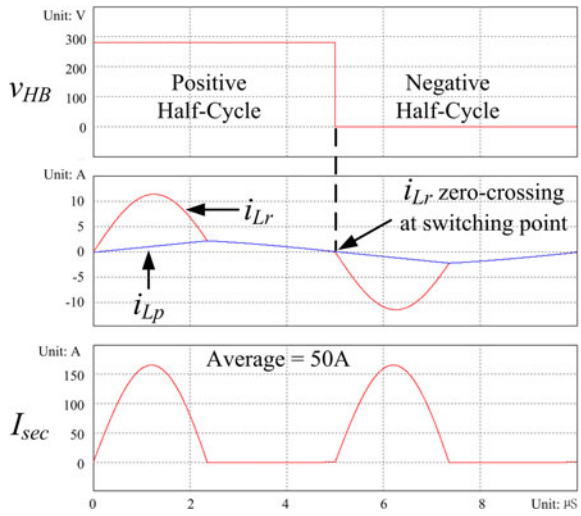

Fig. 13. Peak gain point of Design Example 1. Design No. 25. $V_{\rm in} = 280$ V, $V_o = 12$ V, $F_s = 100$ kHz. Output current is exactly 50 A.

design algorithm—the design candidates have the exact peak gain at the exact minimum switching frequency.

VII. Conclusion

This paper proposes a new approach to find optimal design for *LLC* converters. The core of the proposed approach is an accurate algorithm that can find all the possible designs with the exact peak gain value. The algorithm is derived from time-domain models at the peak-gain point, without any approximation. The equations are established using resonant tank waveforms, law of charge conservation, and conservation of energy. Simulation results show that the proposed algorithm is very accurate.

As will be discussed in Part II of this paper, using the proposed algorithm can eliminate overdesign of the peak gain value and thus minimize the component stress. The resultant candidate designs provide different tradeoffs at different operating conditions. Designers can evaluate the candidate designs and find the optimal design for the targeted application. Design tradeoffs and further studies of the proposed algorithm are presented in Part II of this paper.

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